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PATENT APPLICATION
DOCKET NO.: 200208997-1

REMARKS

Claims 1-23 are currently pending, of which claims 1, 10, and 17 are in independent form.

No claims have been amended.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Claim Rejections - 35 U.S.C. §112, First Paragraph

Claims 1-23 are rejected under 35 U.S.C. §112, First Paragraph, allegedly "as failing to comply with the enablement requirement." With regard to these rejections, the Examiner has stated:

> The specification lacks enablement with respect to the claimed limitation "hot signal" recited in the independent claim 1, 10 and 17. Even though, the definition of a "hot signal" is well known in the art, which may imply an active or live signal while the main power is still on, in this case the specification fails to adequately describe the definition of the hot signal as applied to the claimed invention.
>
> Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. Process Control Corp. v. HydReclaim Corp., 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). In this case, the term "hot signal" in the claims is used by the claims to mean "an encoded signal during

> test", while the accepted meaning is "an active or live signal while the main power is still on." The term is indefinite because the specification does not clearly redefine the term. Therefore, for purpose of examination, the "hot signal" is given a broad interpretation to mean an encoded signal generated from a unit under test, when power is still on.

Applicant respectfully traverses the above enablement rejection and offers the following comments in response. Base claims 1, 10, and 17 do not recite a "hot signal", as the Examiner has asserted, but a "one-hot signal". This term is best explained in the application at Paragraph [0043], *inter alia*, of the present patent application, which describes the generation of the claimed one-hot signals as follows:

> **[0043]** The general operation of a *K*-to-*N* line decoder for generating *N* plurality of one-hot coverage signals based on a *K*-bit input may explained in reference to FIGS. 5B and 5C. A 3-to-8 line decoder 540 receives a 3-bit input 542 that comprises signals a, b and c. The decoder's functionality, which may be implemented using any combination of logic gates, is such that eight 8-bit output signals 544 are generated wherein each signal will be driven high at a particular bit location (i.e., one-hot) for any given logic combination of the three input signals, i.e., a, b and c signals. As shown in the truth table 546 of FIG. 5C [see below], when each of the input signals is a binary 0 (a = b = c = 0), the output 544 is [10000000]. When the input signal combination is such that a = 0, b = 0 and c = 1, the line decoder 540 outputs the signal with the combination [01000000]. Accordingly, when a particular piece of the design under test is modeled as a 3-bit state machine, all the 8 states may be

encoded into a 3-bit signal that is mapped onto a 3-bit bus segment coupled to the 3-to-8 decoder. By examining the output, one can determine whether a particular state has been covered or not during a test sequence. For instance, if the output 544 is [00000010], then the corresponding input must be [110], which implies that the state [110] of the state machine has been covered during test.

One of ordinary skill in the art would recognize that this paragraph describes an encoded signal, e.g., eight signals encoded in three bits, that has been decoded into eight signals each having a single bit asserted according to the table shown in Figure 5C, reproduced here. One skilled in the art would also recognize, from the description and from Figure 5C, that in the decoded signals, only one bit of an eight-bit signal is "hot" or active, hence the description, "one-hot". To the extent that the Examiner has equated a "one-hot signal" to a "hot signal", this interpretation mischaracterizes the term as used in the specification and in the claims. One of ordinary skill in the art would understand the meaning of the term "one-hot" from the

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542 544

Input			Output							
a	b	c	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

FIG. 5C

specification of the present application and would not confuse *N* one-hot signals with *N* hot signals.

For at least the reasons discussed above, Applicant respectfully requests that the pending §112, First Paragraph, rejections be withdrawn.

Regarding the Claim Rejections - 35 U.S.C. §102(b)

The Examiner has rejected claims 1, 9, 16, and 23 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 6,311,303 to Gates et al., hereinafter the *Gates* reference. Applicant notes that base claims 10 and 17, from which claims 16 and 23 respectively depend, are rejected under 35 U.S.C. §103 as discussed below. It is believed that the rejection of dependent claims 16 and 23 under §102(b) was in error, and accordingly, this response assumes that the rejection under §102(b) applies only to claims 1 and 9. In connection with these rejections, the Examiner has commented as follows with respect to base claims 1 and 19:

> Regarding independent Claim 1, Gates discloses methods and interfaces for facilitating testing or debugging of an integrated circuit containing a monitor port with trace bus, several circuit modules and a selection circuit for observing the internal signals for debugging the integrated circuit during the final stages of the integrated circuit design and testing, (integrated circuits 100, 200, 300, as shown in Figs. 1-3, respectively), comprising:

> A selection circuit (tri-state buffers 121 to 11N coupled to a trace select register 150) to select the set of signals from each module (111 to 11N) connected to bus 130 via the associated set of tri-state buffers 121 to 12N, according to expected usefulness of the signals during debugging of the module. The trace select register 150 provides the signals to enable or disable tri-buffers 121 to 12N and thereby select the module that drives internal signals onto bus 130 for output through the monitor port, Fig. 1. In an alternative embodiment of Fig. 2, a multiplexer 220 instead of the tri-state buffers is coupled to the trace select register 150 to select which of module 111 to 11N (i.e., which bus 231 to 23N) drives the output bus 230 of the monitor port.
>
> A line decoder operating to decode the plurality of encoded state coverage signals, as described by Gates, "a decoder (not shown) attached to register 150 decodes the value in register 150 and generates signals that enable selected tri-state buffers 121 to 12N. Aside from the limitation that only one of modules 111 to 11N can drive a line of bus 130 at a time, the decoding of the value in register 150 can enable any combination of tri-state buffers from one or more sets of tri-state buffers 121 to 12N to select a desired combination of internal signals for output through the monitor port". ...

Applicant respectfully traverses the outstanding rejections under §102(b) and offers the following discussion as support. As currently pending, base claim 1 is directed to an embodiment of circuitry for decoding and capturing coverage information. The claimed circuitry is for use with a general purpose performance counter ("GPPC") connected to a bus carrying a plurality of encoded state coverage signals indicative of test coverage in a logic design. The circuitry contains, *inter alia*, a selection circuit

operating to select the plurality of encoded state coverage signals from a multi-bit event signal carried on the bus. A line decoder operates to decode the plurality of encoded state coverage signals into *N* one-hot signals, where each one-hot signal is asserted when a corresponding state in the logic design is covered during a test. A capture circuit is coupled to the line decoder for capturing the *N* one-hot signals. Essentially, the capture circuit accumulates the one-hot signals as a record of test coverage with respect to which states have been covered during the test.

The *Gates* reference is directed to a monitor port connected to selectable output signals from *N* different modules within an integrated circuit that is being monitored. See Abstract. Referring to FIG. 1 of the *Gates* reference, reproduced here, integrated circuit 100 includes circuit modules 111, 112, 113, up to 11N. See column 2, lines 38-43. Two signals are output from monitor port interface 140 on buses 130 and 135. Bus 135 contains common signals that are useful for debugging more

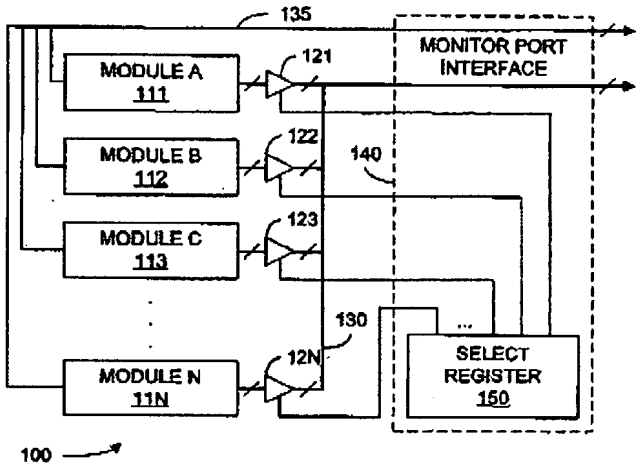

FIG. 1

than one module of circuit 100. See column 3, lines 31-33. Bus 130 contains the output from one of modules 111, 112, 113, through 11N. Select register 150 determines which one of modules 111, 112, 113, through 11N will output signals onto bus 130. See column 2, line 65 through column 3, line 17.

The *Gates* reference discloses that the signals selected and sent via the monitor port interface are internal signals and are useful for debugging the integrated circuit. For a given module that outputs signals onto bus 130, the internal signals can include signals that are received or generated by the module and used only within that module, as well as signals that are generated by the module and sent to other modules or output cells. See column 2, lines 45-57. However, the *Gates* reference does not teach or suggest that the output signals include encoded state coverage signals that are indicative of test coverage. With no encoded state coverage signals present, this reference is hardly concerned with providing a selection circuit operating to select a plurality of encoded state coverage signals from a multi-bit signal carried on the bus, as is recited in claim 1. At best, select register 150 of *Gates* merely provides which module may drive internal signals onto bus 130 rather than selecting a set of encoded state coverage

signals from a bus. See column 2, line 65 through column 3, line 17.

Additionally, although the *Gates* reference mentions a decoder (see column 3, lines 17-25), there is no teaching or suggestion with respect to decoding state coverage signals received from a bus in order to generate one-hot signals indicative of covered states in a logic design under test. Instead, the decoder of the *Gates* reference is merely operable to decode information that has been stored in a register, which is not at all concerned with encoded information sent on a bus. Accordingly, Applicant respectfully submits that it is a mischaracterization to equate the decoder of *Gates* with the claimed line decoder operating to decode a plurality of encoded state coverage signals into *N* one-hot signals.

Based on at least the foregoing analysis, it is believed that independent claim 1 is not anticipated or suggested by the *Gates* reference. Dependent claim 9 depends from base claim 1 and introduces additional features therein. Accordingly, this dependent claim is also believed to be patentable over the applied art of record.

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Regarding the Claim Rejections - 35 U.S.C. §103(a)

Claims 2-8, 10-15, and 17-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the *Gates* reference in view of U.S. Patent No. 6,957,371 to Ricchetti et al. (hereinafter the *Ricchetti* reference). For purposes of the present response, Applicant has assumed that the §103(a) rejections also include dependent claims 16 and 23, as noted earlier. In connection with these rejections, the Examiner has commented as follows with respect to base claims 10 and 17:

> Regarding independent Claims 10, 17, Gates discloses methods and interfaces for facilitating testing or debugging of an integrated circuit containing a monitor port with trace bus, several circuit modules and a selection circuit for observing the internal signals for debugging the integrated circuit during the final stages of the integrated circuit design and testing, (integrated circuits 100, 200, 300, as shown in Figs. 1-3, respectively), comprising:
>
> With respect to claimed limitation of "encoding state coverage information generated when said logic design is under test", integrated circuit 100, Fig. 1, includes several circuit modules (111 to 11N), where each module receives (encoded data) input signals from input cells (not shown) and generate output signals that are useful for debugging integrated circuit 100 during the final stages of integrated circuit design and testing.
>
> A selection circuit (tri-state buffers 121 to 11N coupled to a trace select register 150) to select the set of signals from each module (111 to 11N) connected to bus 130 via the associated set of tri-state buffers 121 to 12N, according to expected usefulness of the signals during debugging of the module. The trace select register

150 provides the signals to enable or disable tri-buffers 121 to 12N and thereby select the module that drives internal signals onto bus 130 for output through the monitor port, Fig. 1. In an alternative embodiment of Fig. 2, a multiplexer 220 instead of the tri-state buffers is coupled to the trace select register 150 to select which of module 111 to 11N (i.e., which bus 231 to 23N) drives the output bus 230 of the monitor port.

A line decoder operating to decode the plurality of encoded state coverage signals, as described by Gates, "a decoder (not shown) attached to register 150 decodes the value in register 150 and generates signals that enable selected tri-state buffers 121 to 12N. Aside from the limitation that only one of modules 111 to 11N can drive a line of bus 130 at a time, the decoding of the value in register 150 can enable any combination of tri-state buffers from one or more sets of tri-state buffers 121 to 12N to select a desired combination of internal signals for output through the monitor port".

A capture circuit (host computer) for capturing the internal signals form the monitor port interface 340, which is connected to host interface 310 via a trace bus 345, selects the internal signals from within host adapter 300 for external monitoring on output balls or pins of a monitor port, by. The monitor port interface 340 is generally for debugging of host adapter 300 during initial design and testing, Fig. 3.

Regarding Claims 2-8,10-15 and 17-22, Gates does not explicitly disclose generating an N-bit mask value stored in a register block for generating an N-bit output. In analogous art, Ricchetti et al. (US Patent No. 6,957,371) discloses a Parallel-To-Serial Conversion (PTSC) circuit 618, which provides Mask Data Out (MDO) signal to the Compare (CMP) circuit 612 to allow the system BIST controller 502 to mask one or more of the expected TDI data bits sent back from the UUT(s).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the masking feature as taught by Ricchetti, in the debugging circuitry of Gates. A person

> skilled in the art would have been motivated to mask such data, when the expected value for a bit of TDI data is indeterminate or unknown logic value. Accordingly, when the MDC signal is asserted in the serial data stream, this signal indicates to the CMP circuit 612 that the result of the corresponding TDO-EDO bit compare is to be ignored, in effect forcing the comparison of the bit to pass, thus saving testing time.

Applicant respectfully traverses the §103(a) rejections of claims 2-8 and 10-23 and submits the following discussion as support. As currently constituted, base claim 10 is directed to a method of capturing state coverage information in a logic design. The claimed embodiment comprises, *inter alia*, encoding state coverage information, generated when the logic design is exercised under test, onto a segment of a bus connected to a general purpose performance counter ("GPPC"). The segment of the bus is selected for processing and decoded into *N* one-hot signals, where each one-hot signal is asserted when a corresponding state in the logic design has been covered during test. The *N* one-hot signals are bit-wise ORed with an *N*-bit mask value stored in a register block to generate an *N*-bit output and the *N*-bit output is selected by a Multiplexer (MUX) block operating under control of at least one control signal. The *N*-bit output is operable to be stored into the register block when selected by said MUX block. Base claim 17 is

a system claim analogous to method claim 10 and contains substantially similar features also.

As discussed with respect to the pending §102 rejections, the *Gates* reference is directed to a monitor port connected to selectable output signals from *N* different modules within an integrated circuit that is being monitored. FIG. 1 of *Gates* discloses integrated circuit 100, including circuit modules 111-11N. Buses 130 and 135 carry two signals that are output from monitor port interface 140. Bus 135 contains common signals that are useful for debugging more than one module of circuit 100. Bus 130 contains the output from one of modules 111-11N. Select register 150 determines which one of modules 111-11N will output signals onto bus 130. To the extent that the claimed operation of encoding state coverage information is being read on the operation of the circuit of the *Gates* reference, Applicant respectfully submits that this reading mischaracterizes the teachings of this reference. As discussed previously, the *Gates* reference does not disclose or suggest state coverage signals that are indicative of test coverage. Further, the *Gates* reference does not discuss encoding test coverage signals or providing state coverage signals indicating those portions of the circuitry that have been exercised.

On the other hand, the pending Office Action appears to assert that modules 111-11N each receive encoded data input. However, the *Gates* reference does not support this assertion. In fact, *Gates* does not disclose the encoding of any type of data, much less of state coverage signals, and the only reference to decoding is the decoder, not shown, that is attached to register 150 and used to determine which module is allowed to output signals.

Therefore, the *Gates* reference is deficient in several respects as applied to base claims 10 and 17. Further, these deficiencies of the *Gates* reference are not cured by the secondary reference, i.e., the *Ricchetti* reference, when combined as a basis for obviousness in the pending Office Action. The *Ricchetti* reference is directed to an embedded electronic system built-in self-test controller that facilitates testing and debugging of electronic circuits. *Ricchetti* does not disclose or suggest the use of state coverage signals and nor is there any teaching or suggestion that such a signal be encoded and output as part of a bus signal. In sum, the combination of the *Gates* and *Ricchetti* references does not teach or suggest all the limitations of base claims 10 and 17.

For at least for the foregoing reasons, it is believed that base claims 10 and 17 as well as the rejected dependent claims (claims 2-8 depending from base claim 1, claims 11-16 depending from base claim 10, and claims 18-23 depending from base claim 17) are in condition for allowance over the combination of the *Gates* reference with the *Ricchetti* reference.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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